Thermal Analysis of Backside Power Delivery Networks (BSPDN)

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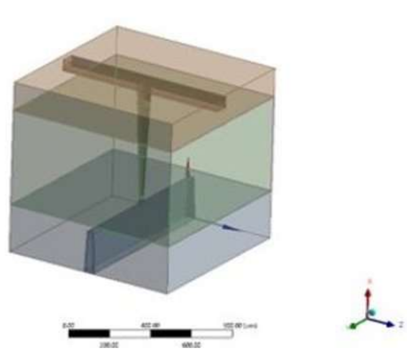
I. Introduction

The purpose of a power delivery network is to provide reference voltage and power to the devices that are on a die. A die is a square of semiconducting material on which an integrated circuit is fabricated. On a traditional wafer, the power delivery network and the signal network are both fabricated on the same front face through back-end of line processing. Back-end of line processing is where individual devices become connected with one another through wiring on the wafer. The problem with the traditional wafers is that the two different networks compete for space on the wafer, which results in congestion of the routing of the signals. On the other hand, the back side of the wafer only serves as a signal transmitting device.

II. Potential Solution and Drawbacks

The idea of the Backside Power Delivery Network configuration is to move the power delivery network to the other side of the chip, the backside. By changing the fabrication order of the chip, there are many improvements. These include direct power delivery to the standard cells of the chip, eliminating the congestion of the different networks on the die, increasing the overall performance of the system, and increasing the utilization of the chip's surface area. In order to connect the power delivery network to the transistors on the backside of the chip, through-silicon vias are used. In order to achieve this, the vias require the extreme thinning of the SI substrate. Thinning can improve the performance and power consumption of microelectronic devices. However, the main concern for the BSPDN concept is the self-heating issues that come with the thinning of the silicon substrate. This issue is what we have been studying.

III. Methods and Future Steps



Before running a thermal analysis on the BSPDN configurations, I needed to create a scaled down version of the larger model. An example model is shown on the right. This model includes the buried power rails (top inner structure), the TSV (middle inner structure), and the backside power delivery network (bottom inner structure) as well as the surrounding silicon materials. I created four types of this structure in the CAD program SolidWorks. Two of the models had a cone-shaped TSV and the other two had a cylindrical-shaped TSV. Furthermore, each group of two was divided into individual distinct models where one had the bottom end of the TSV surrounded by silicon while the other one did not have such attribute. After completing the different models, I began setting up the thermal electrical simulations that used the engineering software ANSYS. The tests that I have ran so far showed that there are minor errors in my CAD models, which prevents the simulations from completely finishing. By fixing the errors in my models, I hope to complete my simulations and obtain useful results that will enable me to form conclusions to our BSPDN analysis.